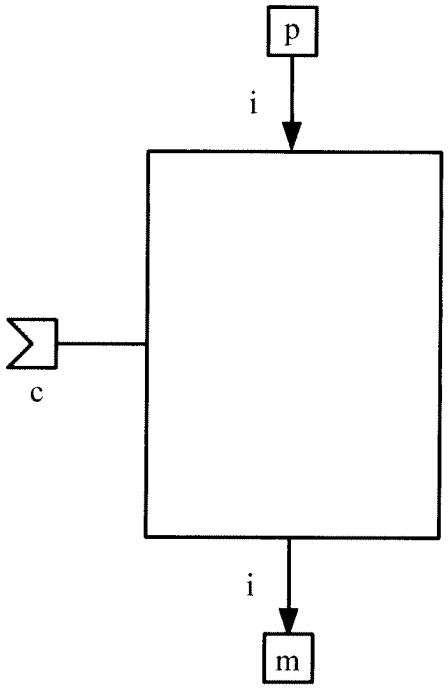


Figure 1A

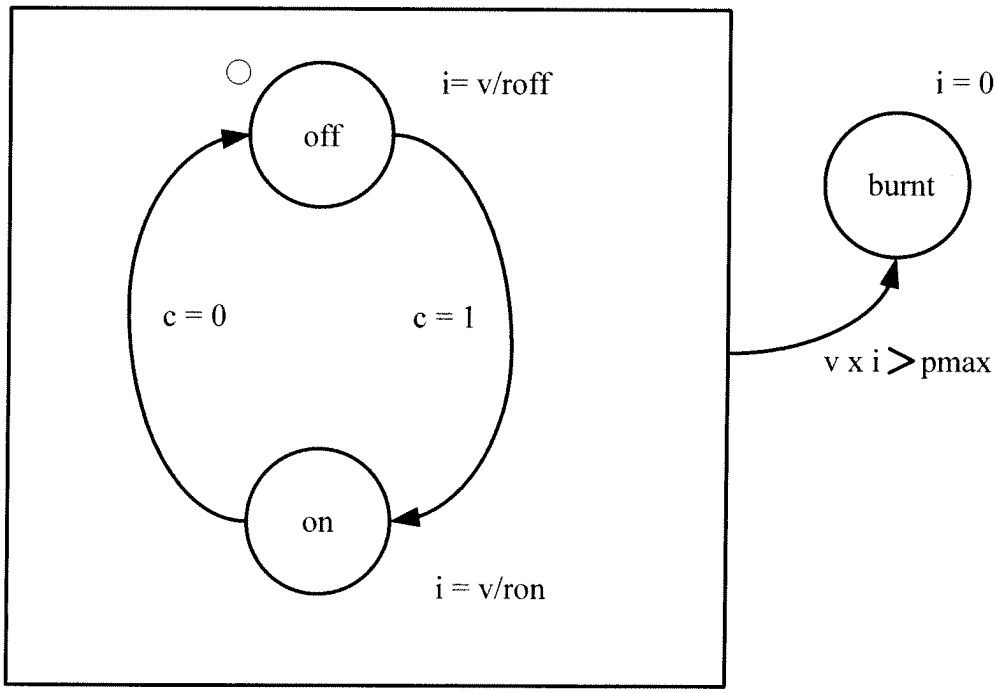


Figure 1B

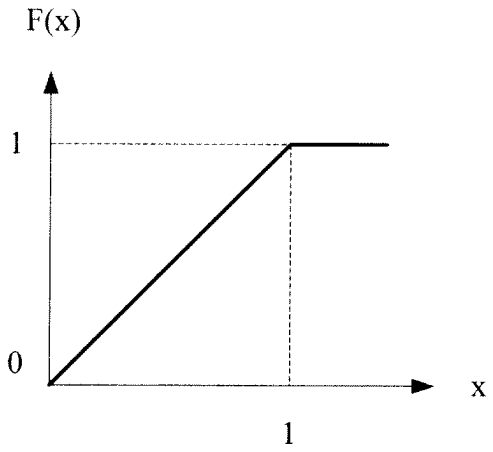


Figure 2A

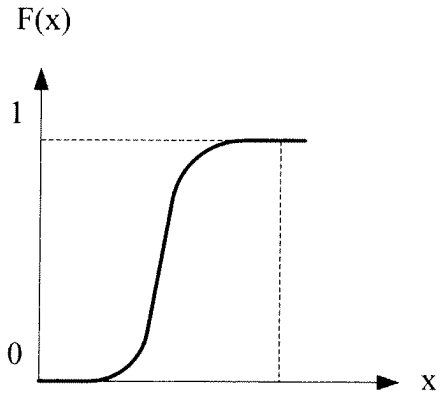


Figure 2B

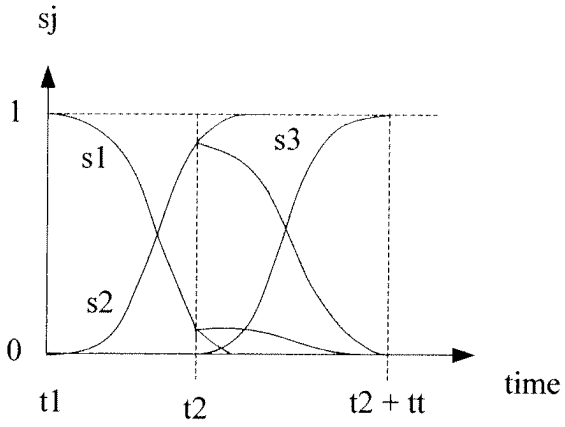


Figure 3A

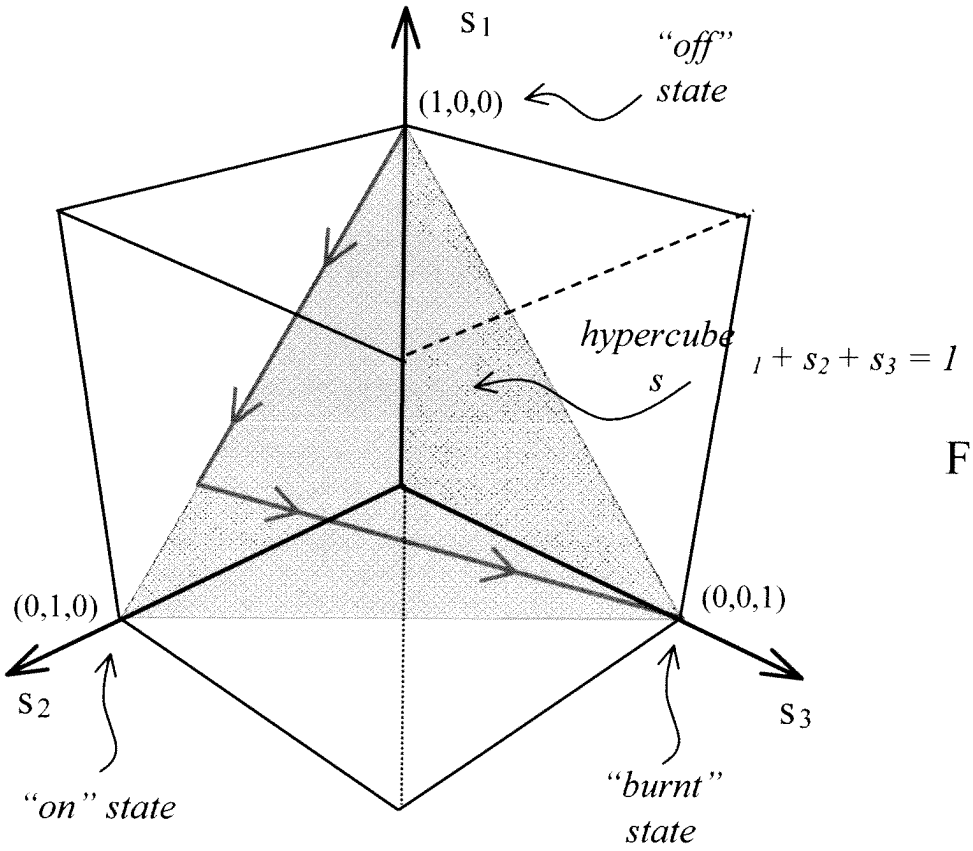
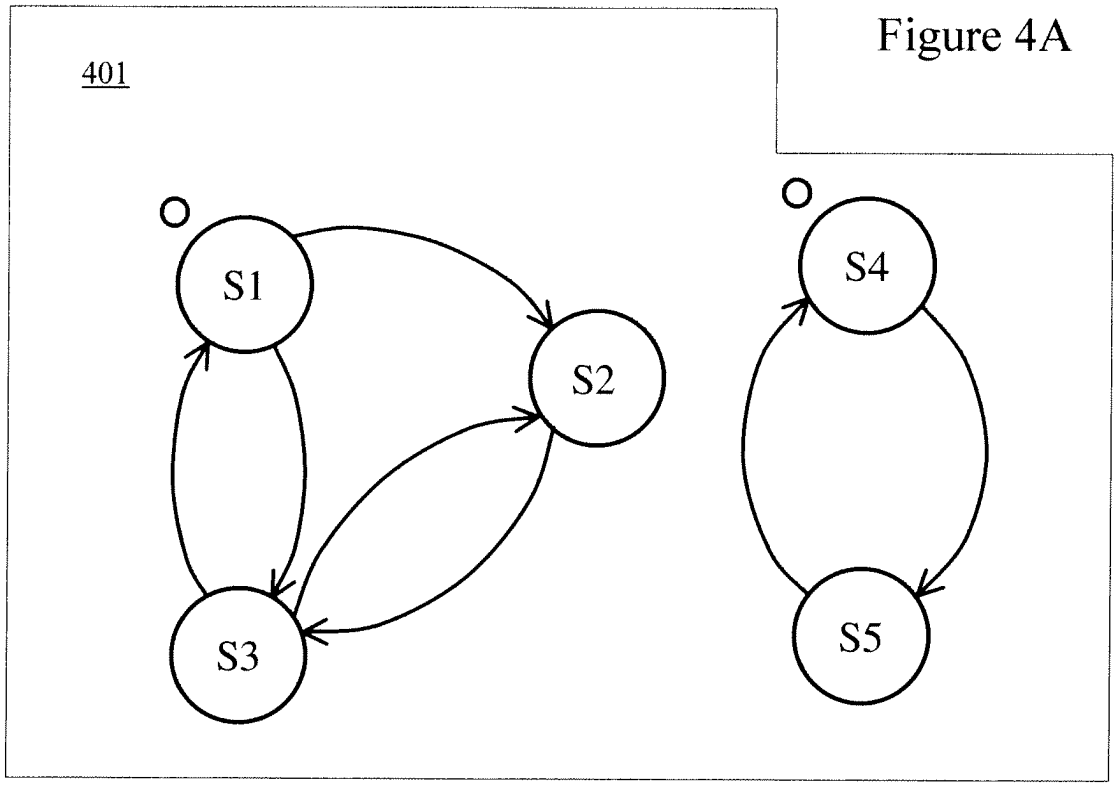


Figure 3B

Figure 4A



state \ variable	x_1	x_2	x_3	x_4
S1				
S2				
S3				
S4				
S5				

402

Figure 4B

variable / combination	x_1	x_2	x_3	x_4
1	S1	S1	S4	S4
2	S1	S3	S4	S4
3	S2	S1	S4	S4
4	S2	S3	S4	S4
5	S1	S1	S5	S5
6	S1	S3	S5	S5
7	S2	S1	S5	S5
8	S2	S3	S5	S5

403

Figure 4C

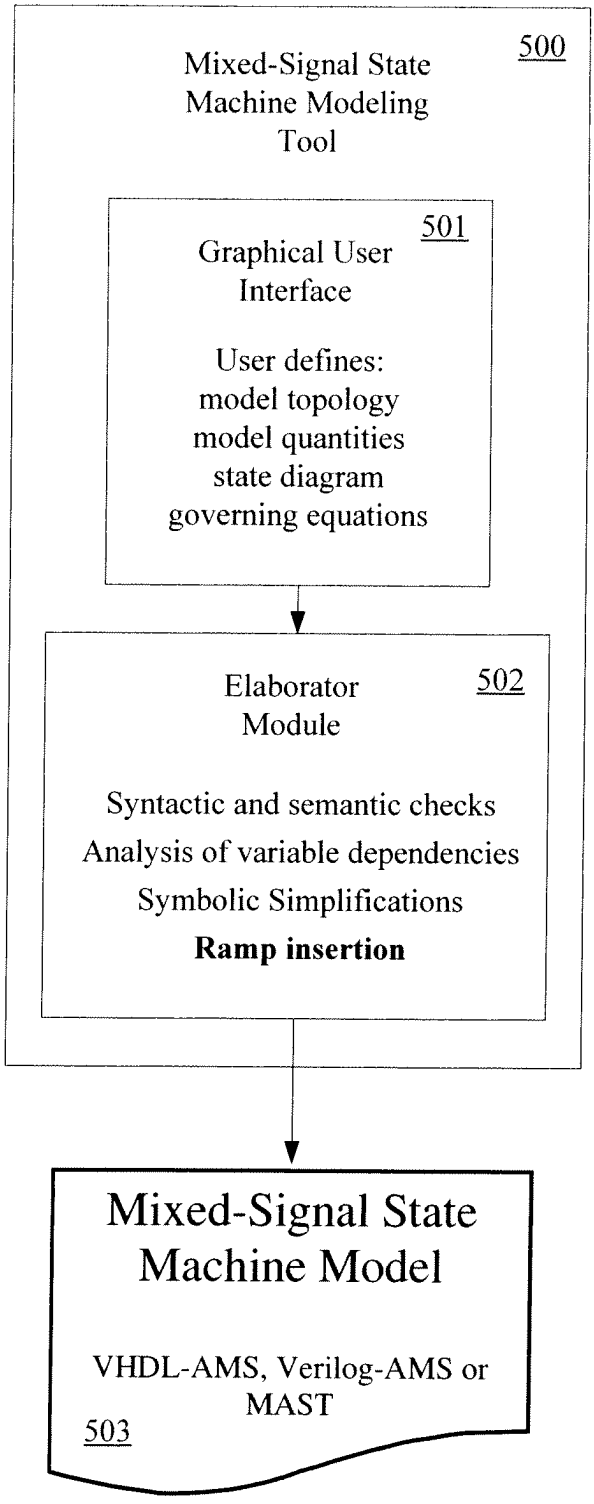

500
Mixed-Signal State Machine Modeling Tool
501
Graphical User Interface
User defines:
model topology
model quantities
state diagram
governing equations
Elaborator Module
502
Syntactic and semantic checks
Analysis of variable dependencies
Symbolic Simplifications
Ramp insertion
Mixed-Signal State Machine Model
VHDL-AMS, Verilog-AMS or MAST
503

Figure 5

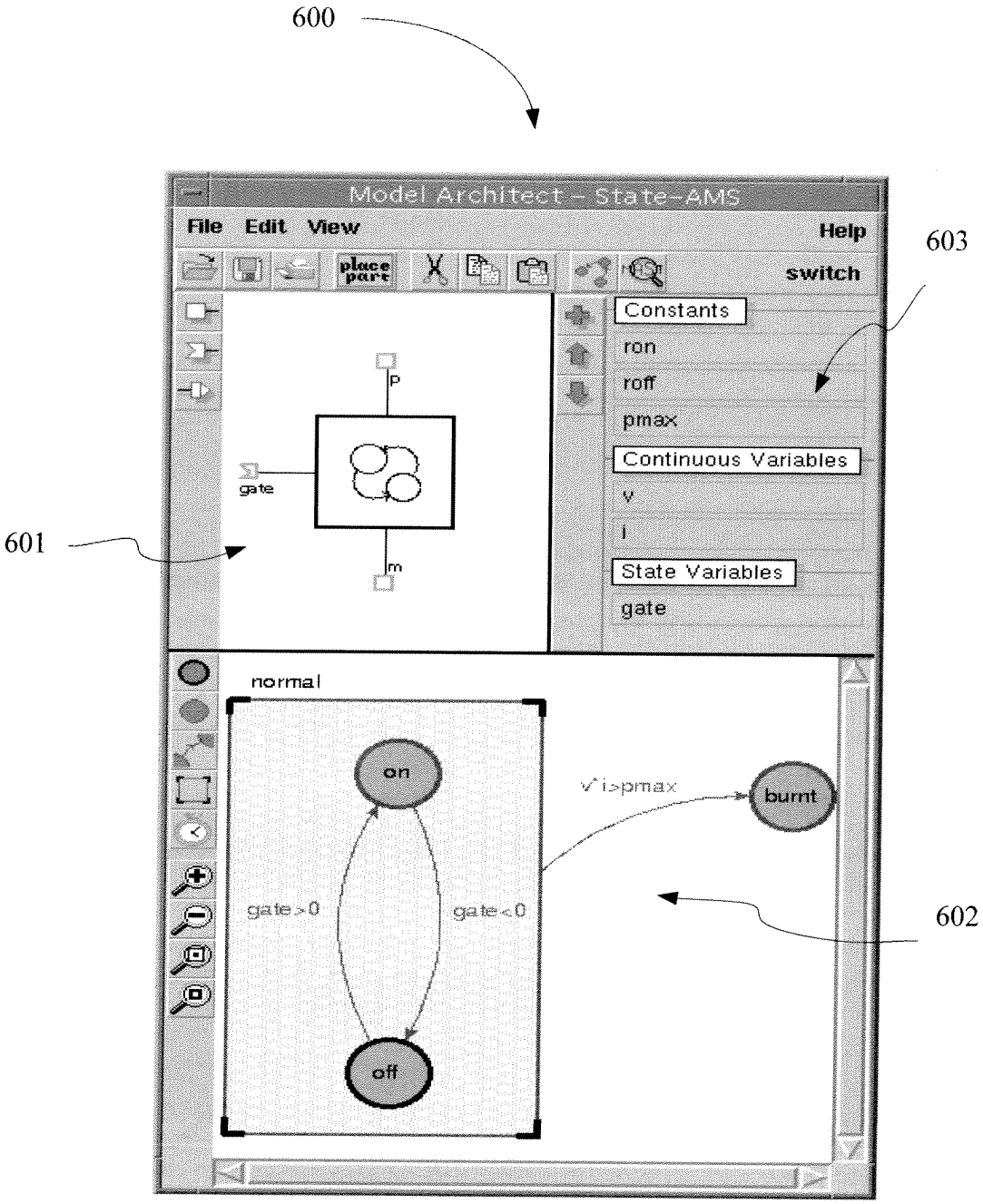

600
Model Architect - State-AMS
File Edit View
Help
place part
switch
603
Constants
ron
roff
pmax
Continuous Variables
v
i
State Variables
gate
601
p
gate
m
normal
on
off
gate>0
gate<0
v^i>pmax
burnt
602

Figure 6A

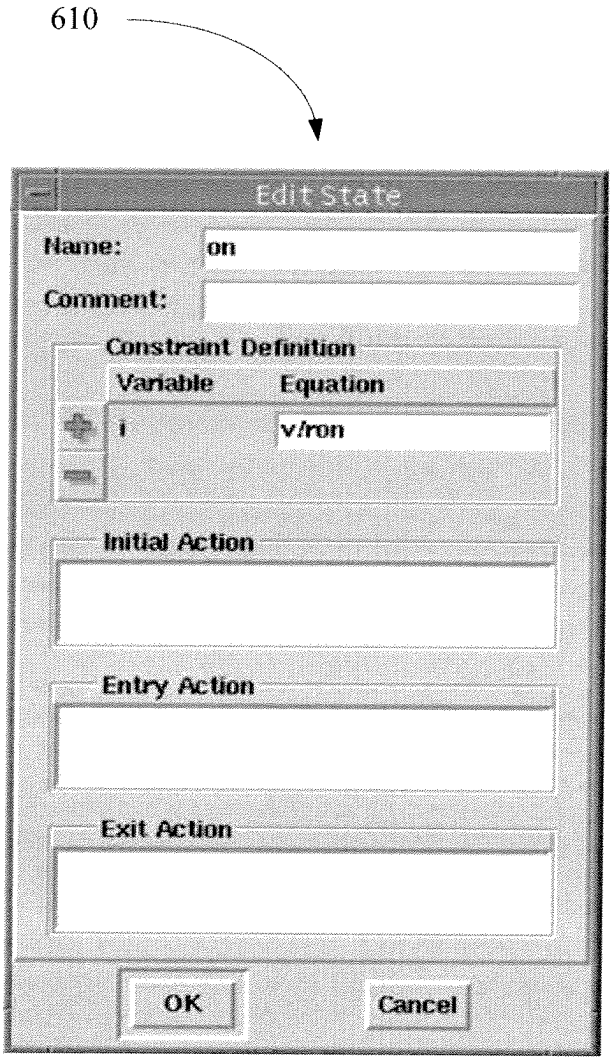

610
Edit State
Name:
on
Comment:
Constraint Definition
Variable
Equation
i
v/ron
Initial Action
Entry Action
Exit Action
OK
Cancel

Figure 6B

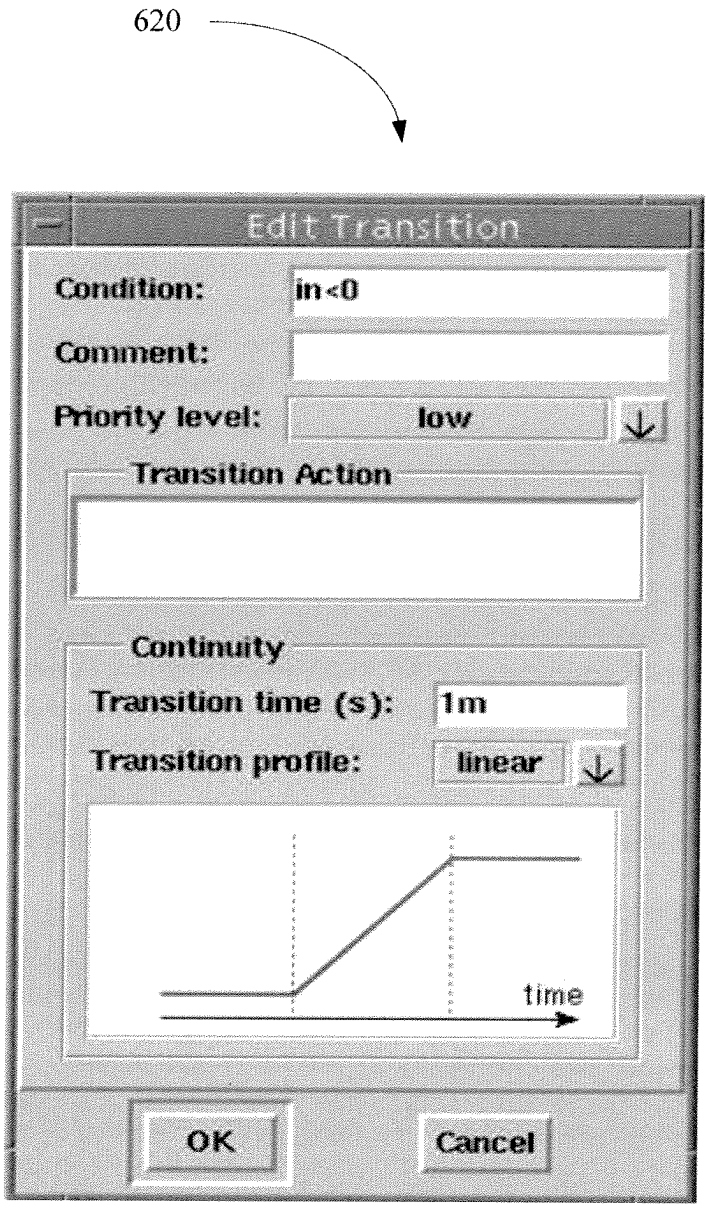

620
Edit Transition
Condition:
in<0
Comment:
Priority level:
low
Transition Action
Continuity
Transition time (s):
1m
Transition profile:
linear
time
OK
Cancel

Figure 6C